IN THE SPECIFICATION

Applicants request that the following paragraphs in the specification be amended as follows:

1) Please replace the paragraph beginning on page 8, line 10, with the following:

FIGS. 6A ~~through 6D~~ through 9D are plan views and cross-sectional views of a semiconductor memory device and a method of manufacturing the same, according to a preferred embodiment of the present invention.

2) Please replace the paragraph beginning on page 10, line 30, with the following:

Thereafter, the third interlevel dielectric layer 234 is deposited on the resultant structure and planarized. The upper level of the third interlevel dielectric ~~layer~~ layer 234 is preferably higher than that ~~of 234~~ of the bit line structure 232. The third interlevel dielectric layer 234 is patterned to form second contact holes (not shown).